SMDP-C2SD Sponsored Workshop on "Recent Trends in VLSI Design"

A one week National Workshop on "**Recent Trends in VLSI Design**" from **16th September 2015 to 23rd September 2015** is organized by Department of ECE & Department of CSE at National Institute of Technology Arunachal Pradesh under the sponsorship of SMDP-C2SD, Department of Electronics & Information Technology, Govt. of India. The outstanding speakers of this workshop are as follows-

1. **Dr. Swapna Banerjee**, Professor, Department of E&ECE, IIT Kharagpur
2. **Dr. Roy P Paily**, Professor, Department of EEE, IIT Guwahati

We got a huge response from our students and faculties as more than **80 candidates** did registration out of which only **45** were given chance to attend the same. The workshop has happened in a flourished way as it has been made interactive by our guest speakers.

Dr. Banerjee discussed more about Digital VLSI where the major topics are VLSI Design Flow, Logic Synthesis & Building Blocks, Logic Hazard Analysis, Logic Testing, Logic Delay Model, Fault Testing, PLA, FPGA, Different Channel Routing, Layout and DRC. Moreover she has discussed about some research problem on Portable Ultrasound, Non-invasive Glucose measurement technique.

Dr. Paily has started discussion from the basics of MOS Physics and he has concentrated more on Analog VLSI. He has discussed on Differential Amplifier, Op-Amp and its applications. Moreover, he has mentioned some of the research problems on Analog & Mixed Signal IC.

So, It is to say that, the workshop is a grand success for the student fraternity.